REMARKS

Applicants respectfully traverse and request reconsideration.

Amendments have been made to the written description to correct typographical errors.

Claims 12-17 and claims 19-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,889,291 to Palanca *et al.* ("Palanca"). Claims 18 stands rejected as being unpatentable over Palanca in view of U.S. Patent No. 6,195,106 B1 to Deering *et al.*

Palanca is directed to a method and apparatus for cache replacement in a multiple variable-way associative cache. (Col. 1, ll. 5-10). As taught, a cache consists of blocks that stores various instructions and data values. The blocks are divided into groups of blocks called sets. In other words, "a set is the collection of cache blocks that a given memory block can reside in. For any given memory block, there is a unique set in the cache that the block can be mapped into, according to present mapping functions. The number of blocks in a set is referred to as the associatively [sic] of the cache, e.g., 2-way set associative means that, for any given memory block there are two blocks in the cache that the memory block[] can be mapped into…." (Col. 1, ll. 19-32). "A cache replacement algorithm determines which cache block in a given set will be evicted." (Col. 2, ll. 17-20) when an eviction is necessary. An eviction of a block in a set is necessary "[w]hen all of the blocks in [the] set for a given cache are full and that cache receives a request, with a different tag address, whether a 'read' or 'write,' to a memory location that maps into the full set." (Col. 1, ll. 52-56).

Independent Claims 12 and 16

Claims 12 and 16 have been amended to clarify the previously presented subject matter. The amendment clarifies the claimed subject matter, specifically, the "previous memory fetch instructions" and the "subsequent memory fetch instruction," and provides that "each of the previous memory fetch instructions and the subsequent memory fetch instruction result in

storage of requested texel information at least in the level one cache." Applicants respectfully submit that no new subject matter has been added in the aforementioned amendment. (*See e.g.*, page 8, line 20- page 10, line 14).

As to both independent claims 12 and 16, the Office Action states that "'overlapping fetched texel information' is data that was fetched from main memory 160 and stored in L2 cache 130, and is thus readily available for a subsequent request in L2 cache for consumption." In support thereof, the Office Action cites Column 4, lines 36-49. However, this position ignores claim language directed to the previous and subsequent memory fetch instructions. While the cited portion of Palanca teaches that "L2 cache 130 acts as an intermediary between main memory 160 and L1 cache 120, and has greater storage ability than L1 cache 120, but may have slower access speed" and that the "[l]oading of data from main memory 160 into multi-processor device 110 goes through L2 cache 130", the cited portions of Palanca appear to be silent as to the "previous memory fetch instructions" and the "subsequent memory fetch instruction" as used in Applicants' claim 1. As amended, each of the previous memory fetch instructions and the subsequent memory fetch instruction result in storage of requested texel information at least in the level one cache.

More specifically, Applicants note that claim 12 requires a level two cache that comprises "overlapping fetched texel information resulting from execution of previous memory fetch instructions" and that the "the level two cache is operative to transmit the overlapping fetched texel information requested by the subsequent memory fetch instruction to the level one cache" when the level one cache does not comprises overlapping fetched texel information requested by a subsequent memory fetch instruction. (Emphasis added). As amended above, the previous memory fetch instructions result in storage of requested texel information at least in the level one cache. Similarly, the subsequent memory fetch instruction results in storage of requested texel information at least in the level one cache.

In contrast to the claimed subject matter, the cited portion of Palanca merely states that the loading of data from main memory into multiprocessor device goes though the L2 cache. It fails to provide for the distinction between previous memory fetch instructions and subsequent memory fetch instructions as claimed. The fact that Palanca teaches that the L2 cache acts as an intermediary between main memory and the L1 cache does not appear to teach or suggest Applicants' claimed interaction with previous memory fetch instructions and a subsequent memory fetch instruction. At best, Palanca teaches the use of a single instruction that requires the temporary storage of requested data in the L2 cache.

Because the current Office Action does not address claim language clarifying the nature of the "previous memory fetch instructions" and the "subsequent memory fetch instruction," and because the cited prior art fails to teach or suggest these claim features, Applicants respectfully submit that claims 12 and 16 are in proper condition for allowance.

Dependent Claims

Claims 13-15 and 17-22 depend upon allowable claims 12 and 16 and further contain additional novel and non-obvious subject matter not disclosed or suggested by the cited prior art. For at least this reason and those cited above with respect to claims 12 and 16, claims 13-15 and 17-22 are further believed to be allowable.

Accordingly, Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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